REMARKS

Applicants appreciate the Examiner's thorough consideration provided the present application. Claims 1, 3-7 and 9-12 are now present in the application. Claims 1 and 7 have been amended. Claims 2 and 8 have been cancelled. Claims 1 and 7 are independent. Reconsideration of this application, as amended, is respectfully requested.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over FIG. 1B of Applicant's Disclosure, in view of Hiraoka, U.S. Patent Application Publication No. US 2004/0100752. This rejection is respectfully traversed.

In light of the foregoing amendments to the claims, Applicants respectfully submit that this rejection has been obviated and/or rendered moot. As the Examiner will note, independent claims 1 and 7 have been amended to recite a combination of elements including "said first gate being disposed on a first side of said bias voltage control terminal" and "said second gate being disposed on a second side of said bias voltage control terminal opposite to said first side, said first gate and said second gate being disposed symmetrically to said bias voltage control terminal". Applicants respectfully submit that the above combination of elements as set forth in amended independent claims 1 and 7 is not disclosed nor suggested by the references relied on by the Examiner.

FIG. 1B of Applicant's Disclosure shows a differential variable capacitor including two independent capacitors 1 and 2. FIG. 1B of Applicant's Disclosure fails to show an integrated design of a differential variable capacitor as recited in claims 1 and 7.

Hiraoka discloses a variable capacitor element in FIG. 6B. Hiraoka also discloses a frequency control terminal 207 connected to the n-type buried electrode layer terminal 201c (see FIG. 2A and 3A; paragraph [0038], lines 15-17; paragraph [0043], lines 16-18). The n-type buried electrode layer terminal 201c corresponds to the wire layer 114 connected to the n-type buried electrode layer 102 in FIGs. 1A and 1B (see paragraph [0030], lines 4-7).

However, Hiraoka fails to teach how the frequency control terminal 207 is arranged with the first and second gates 304 and 309 (or 104 and 109 in FIG. 1B). Therefore, Hiraoka fails to teach that the first and second gates 304 and 309 are disposed on a first side of the frequency control terminal 207 and a second side of the frequency control terminal 207 opposite to the first side. Hiraoka also fails to teach the first and second gates 304 and 309 are disposed symmetrically to the frequency control terminal 207 as recited in claims 1 and 7.

To further clarify the present invention, Applicants respectfully submit that the present invention provides for a symmetrical arrangement of the first and second gates to the bias voltage control terminal to prevent the asymmetric interconnections of the differential capacitor. This feature is not shown in the utilized references.

Accordingly, neither of the references utilized by the Examiner individually or in combination teaches or suggests the limitations of amended independent claims 1 and 7 or their dependent claims. Therefore, Applicants respectfully submit that claims 1 and 7 and their dependent claims clearly define over the teachings of the references relied on by the Examiner.

Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103 are respectfully requested.

CONCLUSION

It is believed that a full and complete response has been made to the Office Action, and that as such, the Examiner is respectfully requested to send the application to Issue.

In the event there are any matters remaining in this application, the Examiner is invited to contact Joe McKinney Muncy, Registration No. 32,334 at (703) 205-8000 in the Washington, D.C. area.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), the Applicants respectfully petition for a one (1) month extension of time for filing a response in connection with the present application and the required fee of $120.00 is attached herewith.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,
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